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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,105	03/16/2001	Noriaki Sakamoto	10417-066001	9488

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CHRIS T. MIZUMOTO
Fish & Richardson P.C.
Suite 2800
45 Rockefeller Plaza
New York, NY 10111

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/810,105	Sakamoto et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 15, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3 and 5-16* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3 and 5-16* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al (US Pat. 5976912) in view of Fjelstad (US Pat. 6001671) and Kweon et al (US Pat. 5900676).

Regarding claim 1, Fukutomi et al disclose a semiconductor device comprising:

- a plurality of conductive paths (63/64, central die pad/support region and 69 in Fig. 22g) which are electrically separated from one another by a trench (66 in Fig. 22a-g)
- a semiconductor chip (65 in Fig. 22g) coupled to a first conductive path (central die pad/support region-not numerically referenced in Fig. 22g) of the plurality of conductive paths having a die pad shape, the chip being coupled/directly connected/fixed through a conventional die bonding material (Col. 23, line 40;)

- the second conductive path having a bonding pad shape (64 region outside the edge portion of the chip in Fig. 22a-g) being formed peripherally around/outside the chip and an external connecting pad (69 in Fig. 22f/g) is provided through the wiring extended from the second conductive path to the rear surface of the chip

-a third conductive path having a shape of an external connecting pad (69 in Fig. 22f/g; Col. 23, line 55) coupled to the second conductive path, the third conductive path being disposed underneath the chip and coupled to the chip through an insulating material

- connecting means such as metallic bonding wires (67 in Fig. 22g) for electrically connecting bonding electrode of the chip and a second conductive path having a bonding shape pad/pattern (64 in Fig. 22a-g; Col. 22, line 33)

- an insulating resin/bonding material covering the chip, embedded/filling in the trench (68/66 in Fig. 22a-g) integrally supporting the conductive paths with their bottom surfaces being exposed

(Fig. 22g; Fig. 22a-g; Col. 22, line 25- Col. 24, line 10).

Fukutomi et al fails to specify coupling the chip using a thermally conductive material.

However, Fukutomi et al further disclose using a conventional die bonding material such as silver paste/thermally conductive paste, tape, etc (Col. 9, line 13; Col. 15, line 13).

Fjelstad teaches using conventional thermally conductive adhesive for coupling the chip to a conductive path (135 in Fig. 1c; Col. 4, line 35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a thermally conductive coupling material so that heat dissipation can be improved using Fjestad's bonding structure in Fukutomi et al's device.

Regarding claim 2, as explained above for claim 1, Fukutomi et al further disclose the first conductive path (central die pad/support region-not numerically referenced in Fig. 22g) having smaller size than that of the rear surface of the chip and a third conductive path having a shape of an external connecting pad (69 in Fig. 22f/g; Col. 23, line 55) provided through the wiring extended from the second conductive path to the rear surface of the chip but fail to specify the third conductive path having a larger size than that of the second conductive path.

Fukutomi et al further disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55). It is a matter of a design choice to select the dimensions/shape of the wiring/electrode layers such as length/width, pad/island area, thickness, etc. of in chip packaging and interconnection technology art to achieve the desired electrical resistance and bonding yield.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the size of third conductive path being larger size

than that of the second conductive path so that the desired electrical resistance and bonding yield can be achieved in Fukutomi et al's device in view of Fjelstad.

Regarding claim 3, Fukutomi et al disclose the third conductive path (69 in Fig. 22f/g; Col. 23, line 55) provided between the periphery of the chip and the first conductive path but fail to specify the second conductive path being in the form of an island.

As explained above for claims 1 and 2, Fukutomi et al disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55). It is a matter of a design choice to select the dimensions/shape of the wiring/electrode layers such as length/width, pad/island area, thickness, etc. of in chip packaging and interconnection technology art to achieve the desired electrical resistance and bonding yield.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select one of the second conductive path in the form of an island so that the desired electrical resistance and bonding yield can be achieved in Fukutomi et al's device in view of Fjelstad.

Regarding claim 5, Fukutomi et al further disclose the insulating/bonding material (68/66 in Fig. 22 g) being provided between the wiring extended to the rear surface of the chip.

Regarding claim 6, Fukutomi et al disclose the insulating/bonding material (68/66 in Fig. 22 g) being provided over the entire region of the rear surface of the chip.

Regarding claim 7, Fukutomi et al disclose the connecting means such as metallic wires (67 in Fig. 22g).

Regarding claim 8, Fukutomi et al disclose forming the wiring patterns/islands using conventional photo resist processing (Col. 22, line 33; Col. 23, line 55) but fail to specify the side of each of the conductive paths being curved to mate with the insulating resin.

Fjelstad teaches forming curved sides of conductive wiring/paths mating with the insulating resin (Fig. 7E-7G; Col. 8) to improve the resin adhesion and bonding.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the side of each of the conductive paths being curved to mate with the insulating resin so that the resin adhesion and bonding can be improved using Fjelstad's wiring design in Fukutomi et al's device.

Regarding claim 9, Fukutomi et al further disclose the conductive paths made of a conductive foil/sheet selected from conventional material such as copper, nickel, etc.

(Col. 22, line 33) but fail to specify selecting the conductive foil from a group consisting of aluminum and iron-nickel.

It is conventional in chip packaging and interconnection technology art to form conductive path/pattern using material such as copper, aluminum, etc. to achieve the desired electrical resistance.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive paths made of a conductive foil/sheet selected from a group consisting of copper, aluminum and iron-nickel to achieve the desired electrical resistance in Fukutomi et al's device.

Regarding claims 10 and 11, Fukutomi et al disclose the upper surface of the conductive path (63 in Fig. 22a-g) being selectively covered/patterned with a different metallic material/film (64 in Fig. 22a-g) such as nickel, gold, etc (Col. 23, line 28) using conventional processes.

Regarding claim 12, Fukutomi et al further disclose forming the conductive solder patterns/bumps for mounting the devices on external wiring/mounting board but fail to specify the same for the first conductive path.

Kweon et al teach conventional mounting/coupling of the die pad/first conductive path having conductive pattern with a wiring/mounting board (300 in Fig. 14; Col. 7, line 1-20) through solder plated/thermally conductive material (150 in Fig. 13-15).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to couple the first conductive path with a conductive pattern formed on the mounting board through a thermally conductive material so that heat dissipation can be improved using Kweon's mounting structure in Fukutomi et al's device in view of Fjelstad.

Regarding claim 13, as explained above for claims 1 and 3, Fukutomi et al disclose forming the wiring patterns/islands and external connecting pads using conventional photo resist processing and solder printing (Col. 22, line 33; Col. 23, line 55) but fail to specify the conductive island of the second conductive path being a test pin.

Kweon et al teach forming the second conductive pad/path in the form of a conventional pin/lead or column (24 Fig. 3, 15, etc.) to provide an electrical connection, testing and external connection requirements for the assembly.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive island of the second conductive path as a test pin so that the electrical testing and rework capability can be

improved using Kweon's pad structure in Fukutomi et al's device in view of Fjelstad.

Regarding claims 14-16, the claim elements are addressed as explained in the above rejections for claim 1.

Response to Arguments

3. Applicant's arguments filed on 04-15-02 have been fully considered but they are not persuasive.

A. Applicant contends that Fukutomi et al do not disclose the conduction path having a die pad shape.

However, as explained above for claim 1, Fukutomi et al disclose the conductive path made of a metallic material such as copper, nickel, etc. which functions as a supporting pad/region for the central part of the die (central die pad/support region in Fig. 22c through g - not numerically referenced) and further provides stability and improved handling during subsequent processing (Col. 23, line 10-30). Therefore, it would be obvious to one of ordinary skill in the art to realize that such die support structure has a die pad shape.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

06-25-02

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800